

WHAT IS CLAIMED IS:

1 1. For use in an operational circuit having a high impedance
2 node, a test circuit capable of connecting said high-impedance node
3 to an external test point when a test signal driving said test
4 circuit is enabled, said test circuit comprising:

5 a first transmission gate switch for coupling said high
6 impedance node to a first internal node of said test circuit when
7 said test signal is enabled, said first transmission gate switch
8 comprising a first N-channel transistor having a drain coupled to
9 said high impedance node, a gate coupled to a Logic 1 when said
10 test signal is enabled, and a source coupled to said first internal
11 node;

12 a second transmission gate switch capable of coupling
13 said first internal node to a second internal node of said test
14 circuit when said test signal is enabled;

15 a third transmission gate switch capable of coupling said
16 second internal node to said external test point when said test
17 signal is enabled; and

18 a biasing circuit for generating a negative V_{GS} bias on
19 said first N-channel transistor when said test signal is disabled
20 to thereby reduce leakage current in said first N-channel
21 transistor.

1 2. The test circuit as set forth in Claim 1 wherein said
2 first transmission gate switch comprises a first P-channel
3 transistor having a drain coupled to said high impedance node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said first internal node.

1 3. The test circuit as set forth in Claim 2 wherein said
2 biasing circuit generates a positive Vgs bias on said first P-
3 channel transistor when said test signal is disabled to thereby
4 reduce leakage current in said first P-channel transistor.

1 4. The test circuit as set forth in Claim 3 wherein said
2 biasing circuit comprises a first impedance circuit coupled between
3 said first internal node and a VDD power supply rail and a second
4 impedance circuit coupled between said first internal node and a
5 ground rail, wherein said first and second impedance circuits form
6 a voltage divider circuit that biases said first internal node to a
7 target bias voltage when said test signal is disabled.

1 5. The test circuit as set forth in Claim 4 wherein said
2 gate of said first N-channel transistor is coupled to a Logic 0
3 when said test signal is disabled and said biasing circuit biases
4 said target bias voltage on said first internal node coupled to
5 said source of said first N-channel transistor to a voltage greater
6 than Logic 0 to thereby generate said negative V_{gs} bias on said
7 first N-channel transistor.

1 6. The test circuit as set forth in Claim 5 wherein said
2 gate of said first P-channel transistor is coupled to a Logic 1
3 when said test signal is disabled and said biasing circuit biases
4 said target bias voltage on said first internal node coupled to
5 said source of said first P-channel transistor to a voltage less
6 than Logic 1 to thereby generate said positive V_{gs} bias on said
7 first P-channel transistor.

1 7. The test circuit as set forth in Claim 6 wherein said
2 second transmission gate switch comprises a second N-channel
3 transistor having a drain coupled to said first internal node, a
4 gate coupled to a Logic 1 when said test signal is enabled, and a
5 source coupled to said second internal node.

1 8. The test circuit as set forth in Claim 7 wherein said
2 second transmission gate switch comprises a second P-channel
3 transistor having a drain coupled to said first internal node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said second internal node.

1 9. The test circuit as set forth in Claim 8 wherein said
2 third transmission gate switch comprises a third N-channel
3 transistor having a drain coupled to said second internal node, a
4 gate coupled to a Logic 1 when said test signal is enabled, and a
5 source coupled to said external test point.

1 10. The test circuit as set forth in Claim 9 wherein said
2 third transmission gate switch comprises a third P-channel
3 transistor having a drain coupled to said second internal node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said external test point.

1 11. A signal generator comprising a phase-locked loop (PLL)
2 circuit capable of generating an output reference signal having a
3 desired frequency, said PLL circuit comprising:

4 a voltage-controlled oscillator;

5 a charge pump and loop filter circuit for generating a
6 control voltage capable of controlling said voltage controlled
7 oscillator; and

8 a test circuit capable of connecting a high-impedance
9 node of said PLL circuit to an external test point when a test
10 signal driving said test circuit is enabled, said test circuit
11 comprising:

12 a first transmission gate switch for coupling said
13 high impedance node to a first internal node of said test
14 circuit when said test signal is enabled, said first
15 transmission gate switch comprising a first N-channel
16 transistor having a drain coupled to said high impedance node,
17 a gate coupled to a Logic 1 when said test signal is enabled,
18 and a source coupled to said first internal node;

19 a second transmission gate switch capable of
20 coupling said first internal node to a second internal node of
21 said test circuit when said test signal is enabled;

22 a third transmission gate switch capable of coupling
23 said second internal node to said external test point when

24 said test signal is enabled; and
25 a biasing circuit for generating a negative Vgs bias
26 on said first N-channel transistor when said test signal is
27 disabled to thereby reduce leakage current in said first N-
28 channel transistor.

1 12. The signal generator as set forth in Claim 11 wherein
2 said first transmission gate switch comprises a first P-channel
3 transistor having a drain coupled to said high impedance node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said first internal node.

1 13. The signal generator as set forth in Claim 12 wherein
2 said biasing circuit generates a positive Vgs bias on said first P-
3 channel transistor when said test signal is disabled to thereby
4 reduce leakage current in said first P-channel transistor.

1 14. The signal generator as set forth in Claim 13 wherein
2 said biasing circuit comprises a first impedance circuit coupled
3 between said first internal node and a VDD power supply rail and a
4 second impedance circuit coupled between said first internal node
5 and a ground rail, wherein said first and second impedance circuits
6 form a voltage divider circuit that biases said first internal node
7 to a target bias voltage when said test signal is disabled.

1 15. The signal generator as set forth in Claim 14 wherein
2 said gate of said first N-channel transistor is coupled to a Logic
3 0 when said test signal is disabled and said biasing circuit biases
4 said target bias voltage on said first internal node coupled to
5 said source of said first N-channel transistor to a voltage greater
6 than Logic 0 to thereby generate said negative V_{gs} bias on said
7 first N-channel transistor.

1 16. The signal generator as set forth in Claim 15 wherein
2 said gate of said first P-channel transistor is coupled to a Logic
3 1 when said test signal is disabled and said biasing circuit biases
4 said target bias voltage on said first internal node coupled to
5 said source of said first P-channel transistor to a voltage less
6 than Logic 1 to thereby generate said positive V_{gs} bias on said
7 first P-channel transistor.

1 17. The signal generator as set forth in Claim 16 wherein
2 said second transmission gate switch comprises a second N-channel
3 transistor having a drain coupled to said first internal node, a
4 gate coupled to a Logic 1 when said test signal is enabled, and a
5 source coupled to said second internal node.

1 18. The signal generator as set forth in Claim 17 wherein
2 said second transmission gate switch comprises a second P-channel
3 transistor having a drain coupled to said first internal node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said second internal node.

1 19. The signal generator as set forth in Claim 18 wherein
2 said third transmission gate switch comprises a third N-channel
3 transistor having a drain coupled to said second internal node, a
4 gate coupled to a Logic 1 when said test signal is enabled, and a
5 source coupled to said external test point.

1 20. The signal generator as set forth in Claim 19 wherein
2 said third transmission gate switch comprises a third P-channel
3 transistor having a drain coupled to said second internal node, a
4 gate coupled to a Logic 0 when said test signal is enabled, and a
5 source coupled to said external test point.